

FIG. 1

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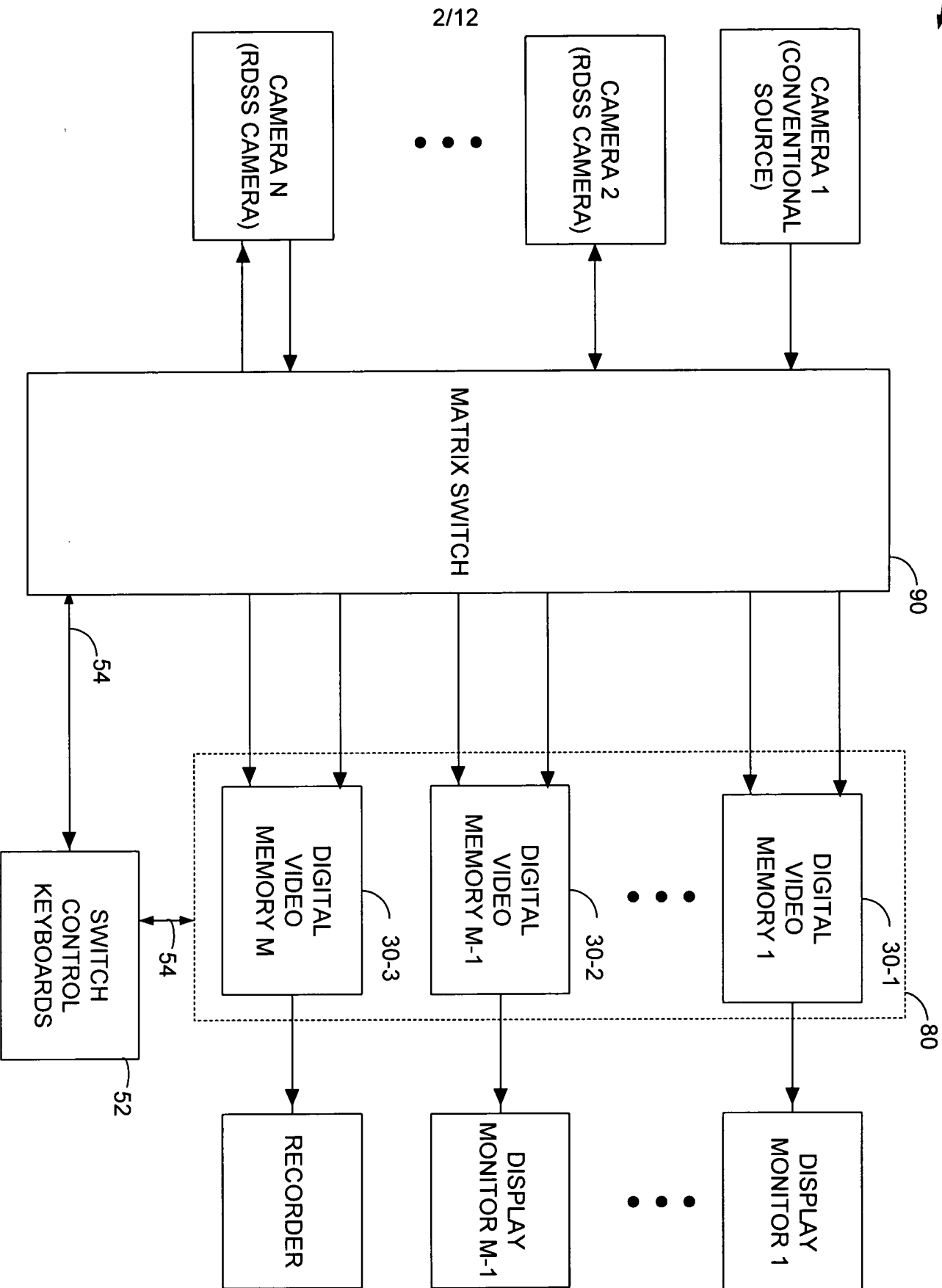
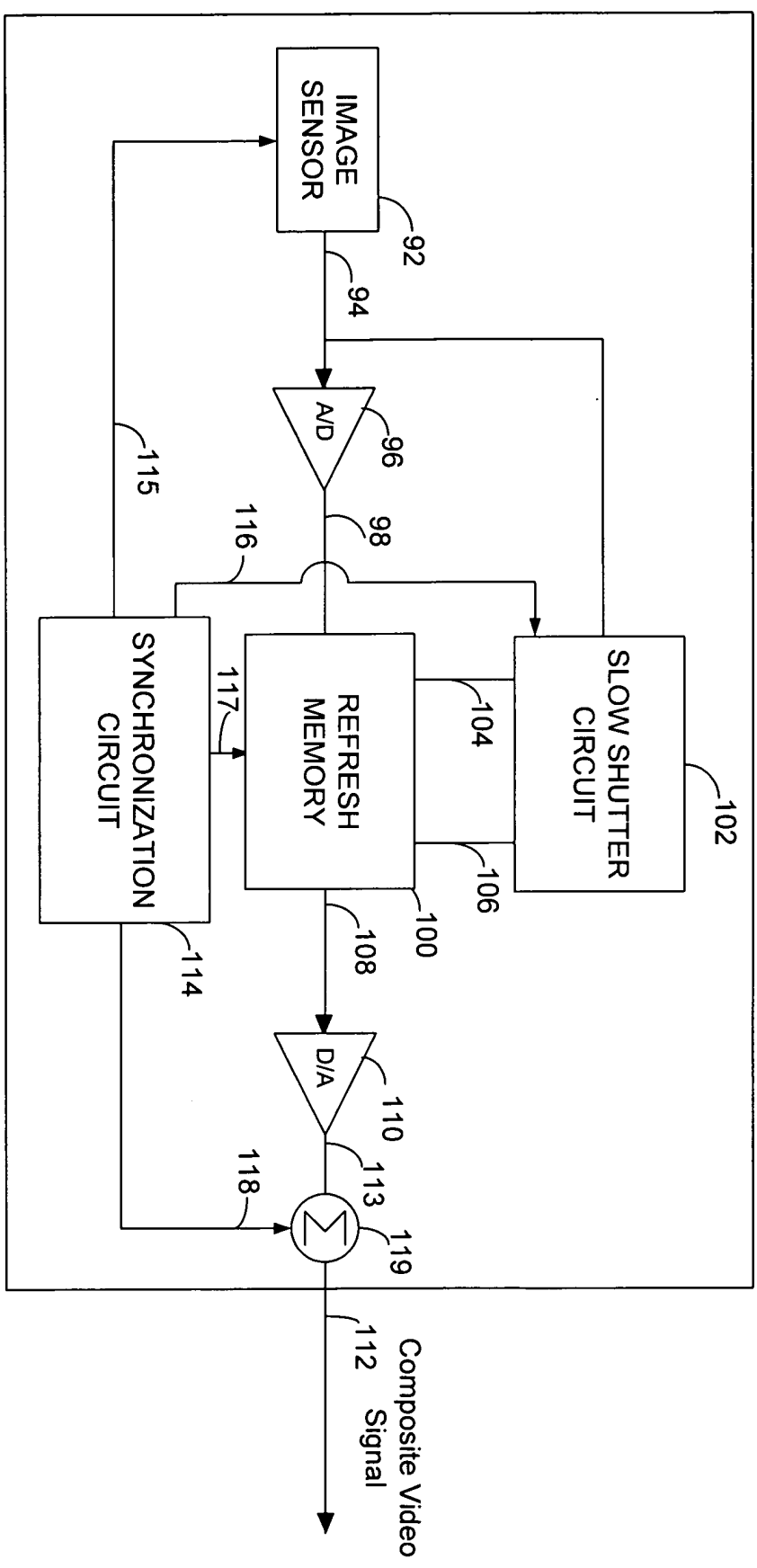


FIG. 2

42-1



CAMERA
FIG. 3

PRIOR ART

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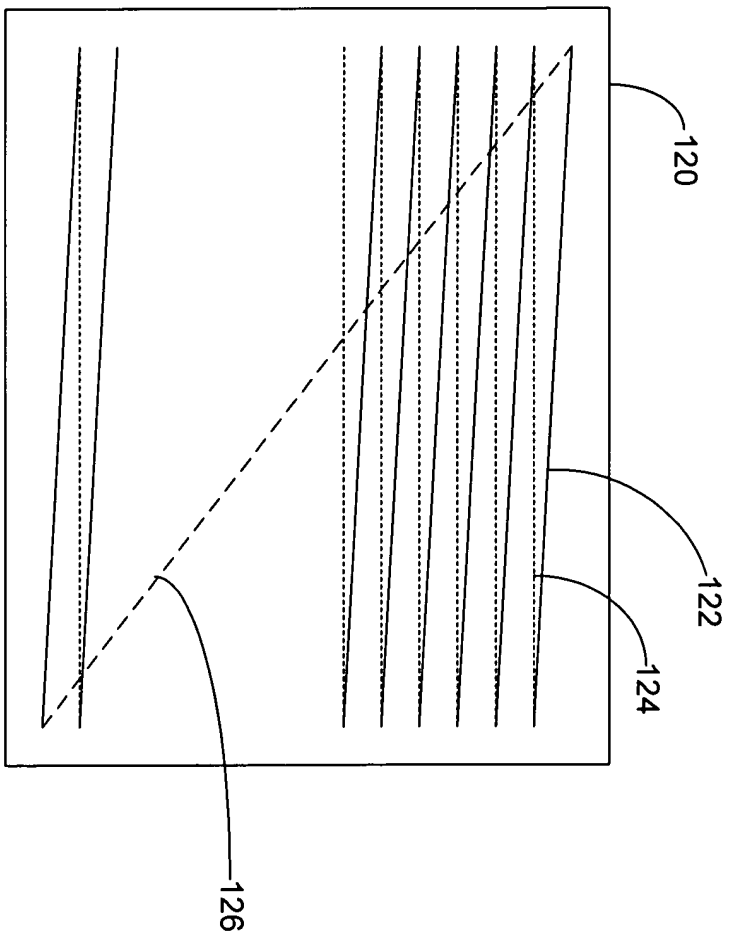


FIG. 4

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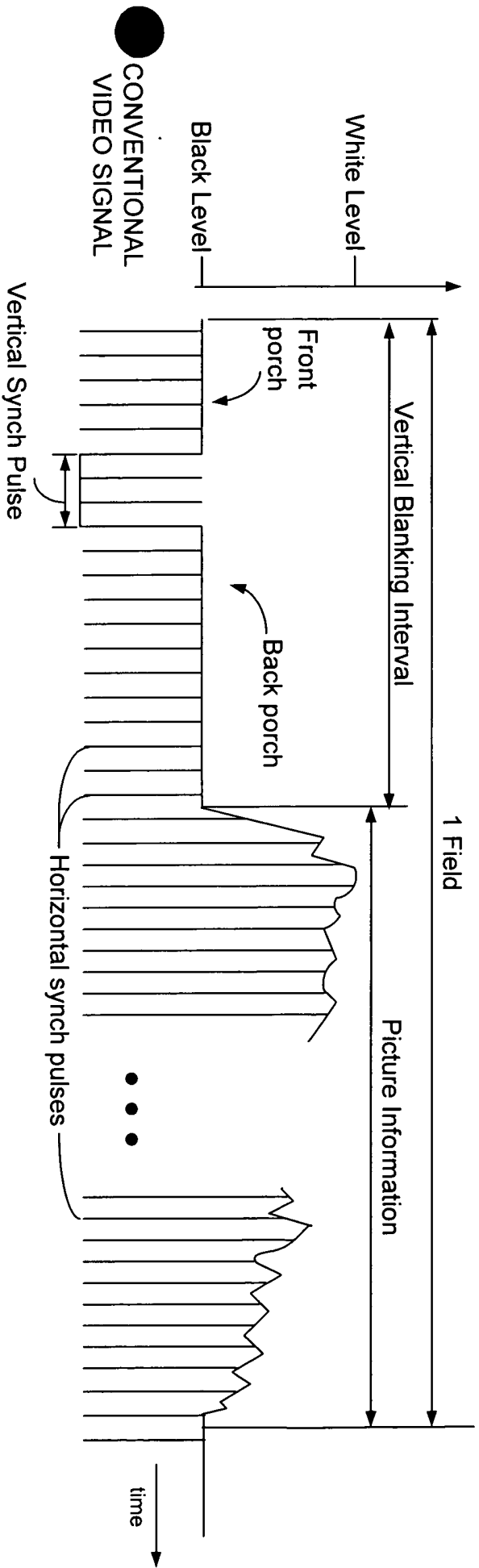
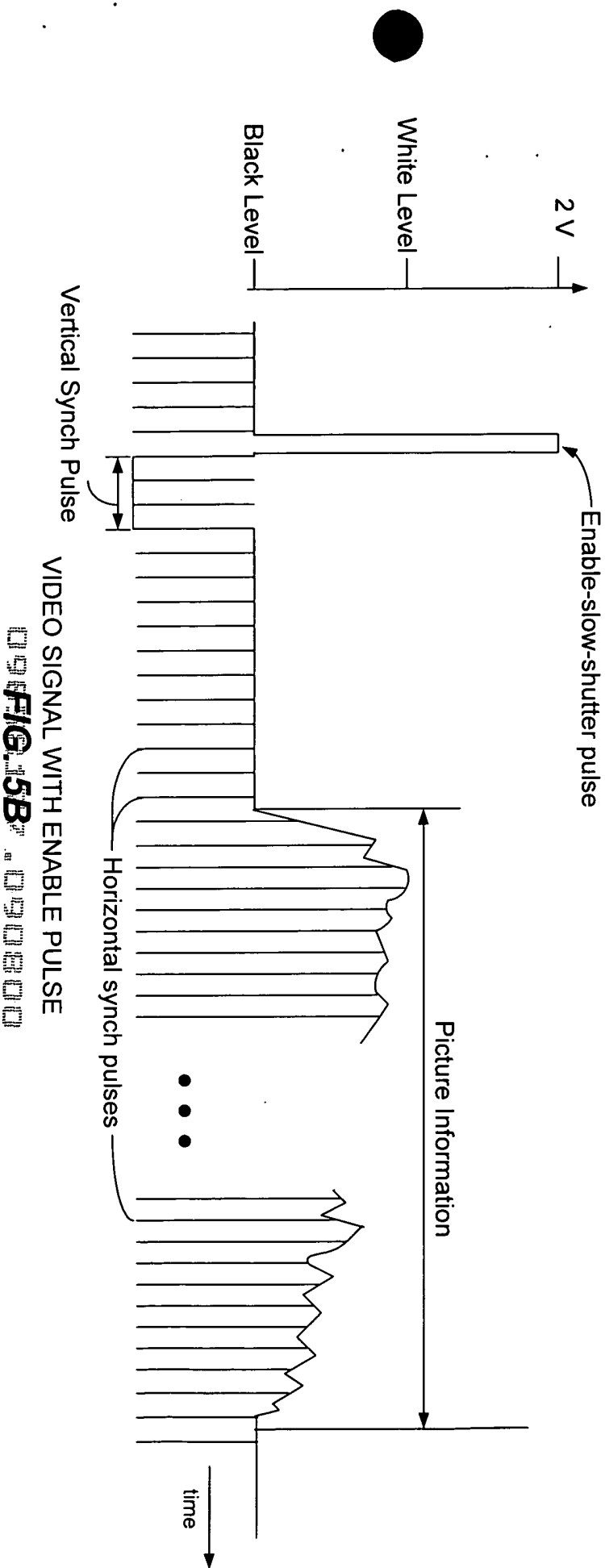
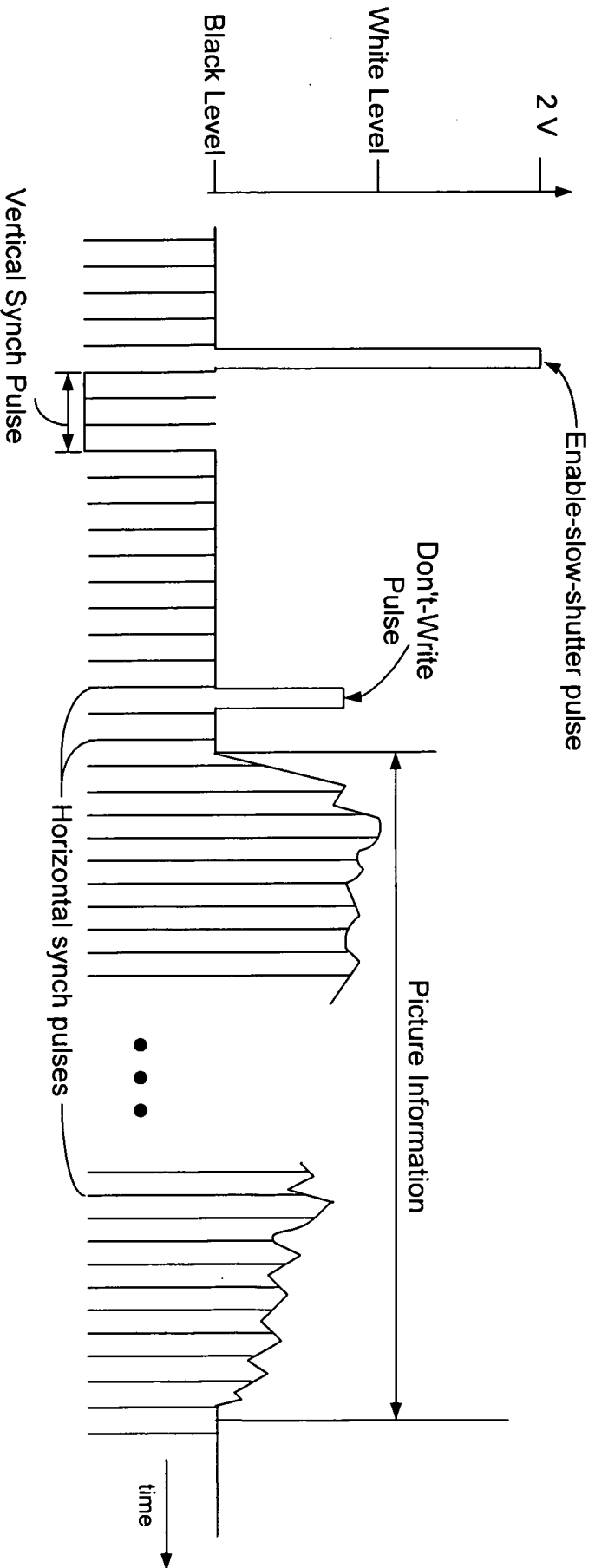


FIG. 5A





VIDEO SIGNAL WITH DONT-WRITE PULSE
FIG. 5C

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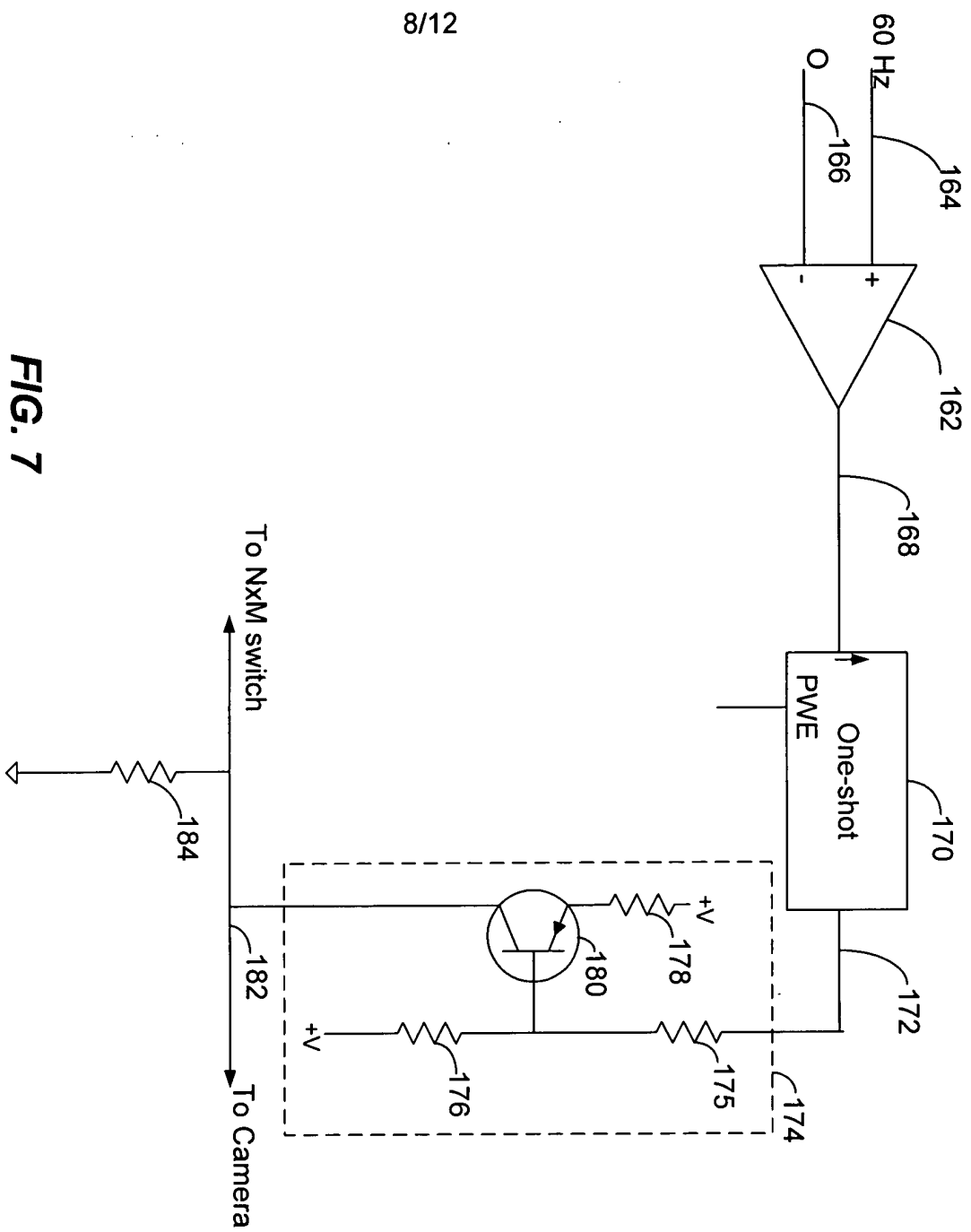
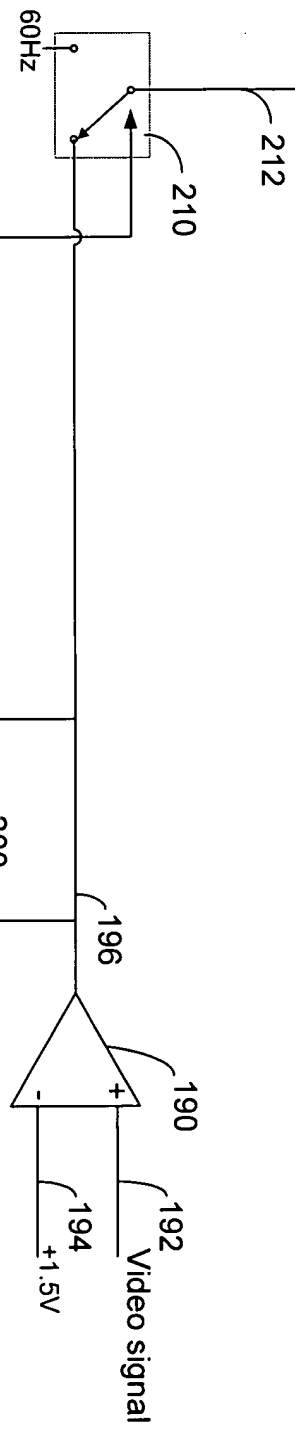


FIG. 7

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CAMERA
SYNCHRONIZER LOCK
CIRCUITS



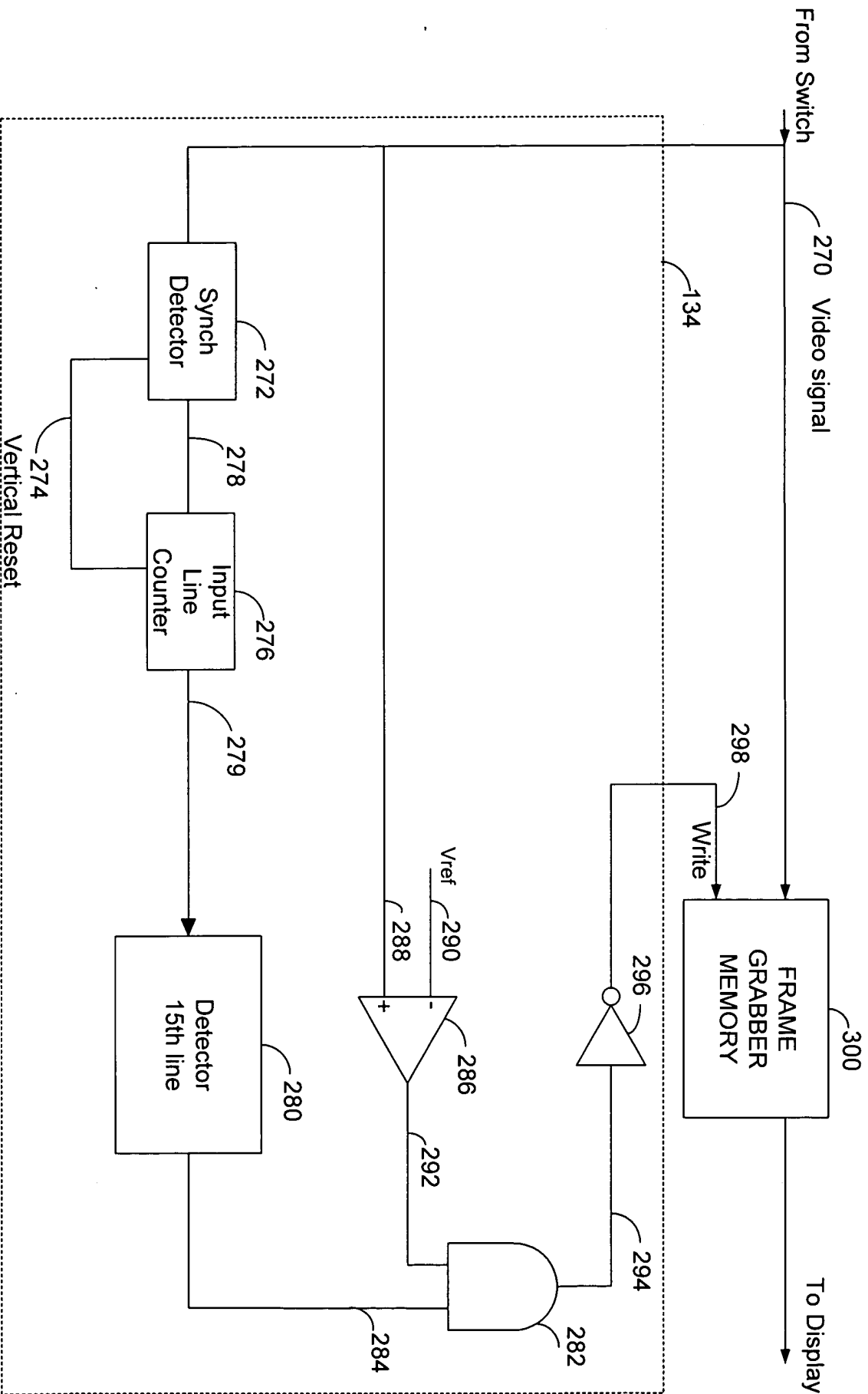
CAMERA

FIG. 8



FIG. 9

00000000000000000000



DIGITAL VIDEO MEMORY WITH THE DETECT-DON'T-WRITE SIGNAL CIRCUIT

FIG. 10

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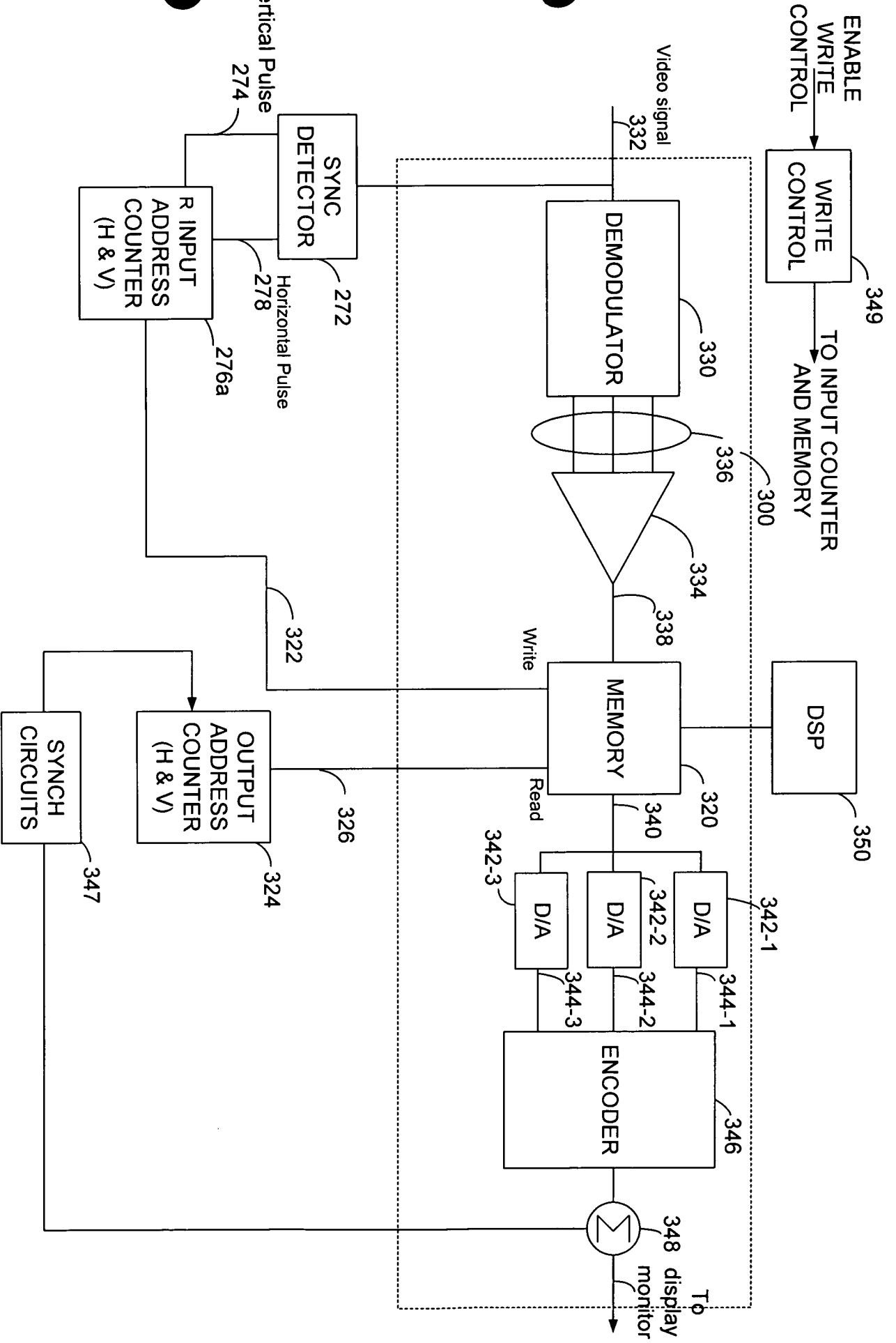


FIG. 11

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